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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/873,038	06/02/2001	Sanjay Lal	004906.P080	4240

8791 7590 10/22/2004

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EXAMINER	
PATEL, HARESH N	

ART UNIT	PAPER NUMBER
2154	

DATE MAILED: 10/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Advisory Action	Application No.	Applicant(s)	
	09/873,038	LAL, SANJAY	
	Examiner	Art Unit	
	Haresh Patel	2154	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 14 September 2004 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE. Therefore, further action by the applicant is required to avoid abandonment of this application. A proper reply to a final rejection under 37 CFR 1.113 may only be either: (1) a timely filed amendment which places the application in condition for allowance; (2) a timely filed Notice of Appeal (with appeal fee); or (3) a timely filed Request for Continued Examination (RCE) in compliance with 37 CFR 1.114.

PERIOD FOR REPLY [check either a) or b)]

a) ☒ The period for reply expires 3 months from the mailing date of the final rejection.

b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.
ONLY CHECK THIS BOX WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

1. ☐ A Notice of Appeal was filed on _____. Appellant's Brief must be filed within the period set forth in 37 CFR 1.192(a), or any extension thereof (37 CFR 1.191(d)), to avoid dismissal of the appeal.

2. ☐ The proposed amendment(s) will not be entered because:

   (a) ☐ they raise new issues that would require further consideration and/or search (see NOTE below);

   (b) ☐ they raise the issue of new matter (see Note below);

   (c) ☐ they are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or

   (d) ☐ they present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____.

3. ☐ Applicant's reply has overcome the following rejection(s): _____.

4. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).

5. ☒ The a)☐ affidavit, b)☐ exhibit, or c)☒ request for reconsideration has been considered but does NOT place the application in condition for allowance because: *See Continuation Sheet*.

6. ☐ The affidavit or exhibit will NOT be considered because it is not directed SOLELY to issues which were newly raised by the Examiner in the final rejection.

7. ☒ For purposes of Appeal, the proposed amendment(s) a)☐ will not be entered or b)☒ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.

   The status of the claim(s) is (or will be) as follows:

   Claim(s) allowed: *None*.

   Claim(s) objected to: *None*.

   Claim(s) rejected: *1-31*.

   Claim(s) withdrawn from consideration: *None*.

8. ☐ The drawing correction filed on _____ is a)☐ approved or b)☐ disapproved by the Examiner.

9. ☐ Note the attached Information Disclosure Statement(s)(PTO-1449) Paper No(s). _____.

10. ☐ Other: _____

JOHN FOLLANSBEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Continuation of 5. does NOT place the application in condition for allowance because: the prior art still renders the claims unpatentable and the final rejection is deemed proper.

As per claims, 1, 12 and 21, Kranich teaches, "a number of instructions at an address within a common interrupt handling vector address space ... wherein the number of instructions cause the processor to determine an idenification of the processor based on a quer that is internal to the processor", col., 22, line 39 - col., 23, line 28. As per claims 8, 17, and 28, Kranich teaches, "a number of instructions at an address within the common interupt handling addess space of the same memory, wherein the number of instructions cause the processor to read a bit within an internal register to determine an identification of a processor in a multiprocesor system", col. 22, line 39 - col., 23, line 28. Kranich also teaches "executing a set of instructions that are within a common interrupt handling vector where one of the instrucitons from within the common interrupt handling vector causes a processor to determine its identification based on a query that is internal to that processor including reading a bit within an internal register of that processor", "the use of a processor that processes queries related to both internal and external to the processor in order to help determine the identifiation of the processor", "a process that queries internal and external processor to determine the identity of the proessor", col., 21, line 21 - col., 22, line 38. In response to the applicant's argument that examiner has not identified Yoshioka that cures the defect of Kranich, Yoshioka clearly teache use of a common interrupt hander (e.g., concept of handling common exception events, figure 2). In response to the applicant's arguemtn that Yoshioka and Kranich are improperly combined, both the cited references Yoshika and Kranich teach what the applicant i trying to accomplish, i.e., the claimed invention by the usage of preambles "a method comprising", "a system comprising", "the machine to perform operations comprising", and, "a method for handling a number of execeptions within a processor in a multi-procesing system Also, The test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of a primary reference. It is also not that the cliamed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinally skill in the art. In re Keller, 642 F.2d 414, 425, 208 USPQ 871, 881 (CCPA 1981); In re Young, 927 F.2d 588, 591, 18 USPQ2d 1089, 1091 (Fed. Cir. 1991). Therefore, Yoshika and Kranich meet the clamied limiations.

As per claims, 1, 12 and 21, Brenner in view of Browning teaches, "a number of instructions at an address within a common interrupt handling veclor address space ... wherein the number of instructions cause the processor to determine an idenification of the processor based on a query that is internal to the processor", e.g., paragraphs 9-11. As per claims 8, 17, and 28, Brenner in view of Browning teaches, "a number of instructions at an address within the common interupt handling addess space of the same memory, wherein the number of instructions cause the processor to read a bit within an internal register to determine an identification of a processor in a multiprocesor system", e.g., paragraphs 4-7. Brenner in view of Browning also teaches "executing a set of instructions that are within a common interrupt handling vector where one of the instrucitons from within the common interrupt handling vector causes a processor to determine its identification based on a query that is internal to that processor including reading a bit within an internal register of that processor", "the use of a processor that processes queries related to both internal and external to the processor in order to help determine the identifiation of the processor", "a process that queries internal and external processor to determine the identity of the proessor", e.g., paragraphs 7-11. In response to the applicant's arguemtn that Brenner and Browning Yoshioka are improperly combined, both the cited references Brenner in view of Browning teach what the applicant is trying to accomplish, i.e., the claimed invention by the usage of preambles "a method comprising", "a system comprising", "the machine to perform operations comprising", and, "a method for handling a number of execeptions within a processor in a multi-procesing system". Also, The test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of a primary reference. It is also not that the cliamed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings o the references would have suggested to those of ordinally skill in the art. In re Keller, 642 F.2d 414, 425, 208 USPQ 871, 881 (CCPA 1981); In re Young, 927 F.2d 588, 591, 18 USPQ2d 1089, 1091 (Fed. Cir. 1991). Therefore, Brenner in view of Browning meet the clamied limiations.

Also, page 13, lines 10 - 18, clearly states "Embodiments of the present invention can provide this exception handling without requiring the processors to determine a processor identification through extemal queries to external devices, such as a memory controller, thereby making the handling of the exceptions faster. Although the present invention has been described with reference to specific exemplary embodiments, it will be evident that various modifications and changes may be made to these embodiments without depming from the broader spirit and scope of the invention. Accordingly, the specification and drawings are to be regarded in an illustrative rather than a restrictive sense". Since, applicant's claims contain broadly claimed subject matter, it clearly reads upon the examiner's interpretation o these actions.

Examiner do understand the applicant's invention, i.e., figures 1-5 of the specification, however the scope of the present claims is too broad that can be interpreted several ways, which reads upon the prior arts. Hence, examiner is making an additional serious effort for amending the indepdent claims.

Applicant is suggested to make the following amendments to the claims to define the scope of their invention and to distinguish over the prior art.

Claim 17:
A system comprising:
multiple processors and an exception handling processor dedicated to handle exceptions of the system;
the multiple processors executes different operating systems;
a memory that includes:
a common exception handling vector address space; and

a number of separate exception handling vector address spaces, each containing a unique interrupt handler for each said different operating systems;

a memory controller coupled to the memory;

the multiple processors and the exception handling processor coupled to the memory controller;

the exception handling processor including an internal register;

upon receiving an exception, a processor of the multiple processors, determines a type of the exception it received and executes instructions at an address within the common exception handling vector address space;

the instructions at the address causes the exception handling processor to determine an identification of the processor based on a value stored in the internal register, and to further execute the respecitve unique interrupt handler for the operating sytem of the identified processor.

Claim 8:

A method comprising steps of:

receiving an exception within a processor; wherein a processor belongs to multiple processors and an exception handling processor dedicated to handle exceptions of the system; wherein, the multiple processors executes different operating systems; wherein a memory includes:

a common exception handling vector address space; and

a number of separate exception handling vector address spaces, each containing a unique interrupt handler for each said different operating systems; wherein, a memory controller is coupled to the memory;

wherein, the multiple processors and the exception handling processor coupled to the memory controller;

wherin, the exception handling processor including an internal register;

determining a type of the exception it received and executes instructions at an address within the common exception handling vector address space;

wherein, the instructions at the address causes the exception handling processor to determine an identification of the processor based on a value stored in the internal register, and to further execute the respecitve unique interrupt handler for the operating sytem of the identified processor.

Claim 28:

A machine-readable medium that provides instructions, which when executed by a machine, causes the machine to perform operations comprising:

receiving an exception within a processor; wherein a processor belongs to multiple processors and an exception handling processor dedicated to handle exceptions of the system; wherein, the multiple processors executes different operating systems; wherein a memory includes:

a common exception handling vector address space; and

a number of separate exception handling vector address spaces, each containing a unique interrupt handler for each said different operating systems; wherein, a memory controller is coupled to the memory;

wherein, the multiple processors and the exception handling processor coupled to the memory controller;

wherein, the exception handling processor including an internal register;

determining a type of the exception it received and executes instructions at an address within the common exception handling vector address space;

wherein, the instructions at the address causes the exception handling processor to determine an identification of the processor based on a value stored in the internal register, and to further execute the respecitve unique interrupt handler for the operating sytem of the identified processor.